WHAT IS CLAIMED IS:

1. A differential difference amplifier for amplifying an input signal close to a negative supply voltage and adding an offset voltage to the amplified input signal, said differential difference amplifier comprising:

a first non-inverting input terminal capable of being coupled to said input signal;

a first inverting input terminal capable of being coupled to said negative supply voltage;

a second inverting input terminal capable of being coupled to a feedback resistor coupled to an output of said differential difference amplifier;

a second non-inverting input terminal capable of being coupled to said offset voltage;

a first differential transistor pair comprising a first transistor having a gate coupled to said first non-inverting input and a second transistor having a gate coupled to said first inverting input;

a second differential transistor pair comprising a third transistor having a gate coupled to said second non-inverting input and fourth transistor having a gate coupled to

said second inverting input;

a first cascode transistor pair comprising a fifth transistor having a gate coupled to said first non-inverting input and a source coupled to a drain of said first transistor and a sixth transistor having a gate coupled to said first inverting input and a source coupled to a drain of said second transistor; and

a second cascode transistor pair comprising a seventh transistor having a gate coupled to said second non-inverting input and a source coupled to a drain of said third transistor and an eighth transistor having a gate coupled to said second inverting input and a source coupled to a drain of said fourth transistor.

2. The differential difference amplifier as set forth in Claim 1 wherein a source of said first transistor and a source of said second transistor are coupled to the output of a first bias current generating source.

3. The differential difference amplifier as set forth in Claim 2 wherein a bulk connection of said first transistor and a bulk connection of said second transistor are coupled to said offset voltage.

4. The differential difference amplifier as set forth in Claim 3 wherein a bulk connection of said fifth transistor and a bulk connection of said sixth transistor are coupled to said sources of said first and second transistors.

5. The differential difference amplifier as set forth in Claim 4 wherein a source of said third transistor and a source of said fourth transistor are coupled to the output of a second bias current generating source.

6. The differential difference amplifier as set forth in Claim 5 wherein a bulk connection of said third transistor and a bulk connection of said fourth transistor are coupled to a positive supply voltage.

7. The differential difference amplifier as set forth in Claim 6 wherein a bulk connection of said seventh transistor and a bulk connection of said eighth transistor are coupled to said sources of said third and fourth transistors.

8. The differential difference amplifier as set forth in Claim 7 wherein a drain current of said fifth transistor and a drain current of said seventh transistor are combined to produce a first composite current.

9. The differential difference amplifier as set forth in Claim 8 wherein a drain current of said sixth transistor and a drain current of said eighth transistor are combined to produce a second composite current.

10. The differential difference amplifier as set forth in Claim 9 further comprising a current difference detection circuit capable of detecting a current difference in said second and first composite currents and generating an output voltage proportional to said current difference.

11. A battery monitoring apparatus comprising:

a sense resistor coupled to a battery such that a charge current flows through said sense resistor when said battery is charging and a discharge current flows through said sense resistor when said battery is discharging;

an offset voltage generation circuit capable of generating an offset voltage;

a differential difference amplifier for amplifying a voltage sense signal on said sense resistor and adding said offset voltage to the amplified voltage sense signal, said differential difference amplifier comprising:

a first non-inverting input terminal capable of being coupled to said voltage sense signal;

a first inverting input terminal capable of being coupled to a negative supply voltage;

a second inverting input terminal capable of being coupled to a feedback resistor coupled to an output of said differential difference amplifier;

a second non-inverting input terminal capable of being coupled to said offset voltage;

a first differential transistor pair comprising a

first transistor having a gate coupled to said first non-inverting input and a second transistor having a gate coupled to said first inverting input;

a second differential transistor pair comprising a third transistor having a gate coupled to said second non-inverting input and fourth transistor having a gate coupled to said second inverting input;

a first cascode transistor pair comprising a fifth transistor having a gate coupled to said first non-inverting input and a source coupled to a drain of said first transistor and a sixth transistor having a gate coupled to said first inverting input and a source coupled to a drain of said second transistor; and

a second cascode transistor pair comprising a seventh transistor having a gate coupled to said second non-inverting input and a source coupled to a drain of said third transistor and an eighth transistor having a gate coupled to said second inverting input and a source coupled to a drain of said fourth transistor; and

an analog-to-digital converter ADC coupled to an output of said differential difference amplifier for converting said

amplified voltage sense signal and said offset signal to a digital signal readable by a processing circuit couple to said ADC.

12. The battery monitoring apparatus as set forth in Claim 11 wherein a source of said first transistor and a source of said second transistor are coupled to the output of a first bias current generating source.

13. The battery monitoring apparatus as set forth in Claim 12 wherein a bulk connection of said first transistor and a bulk connection of said second transistor are coupled to said offset voltage.

14. The battery monitoring apparatus as set forth in Claim 13 wherein a bulk connection of said fifth transistor and a bulk connection of said sixth transistor are coupled to said sources of said first and second transistors.

15. The battery monitoring apparatus as set forth in Claim 14 wherein a source of said third transistor and a source of said fourth transistor are coupled to the output of a second bias current generating source.

16. The battery monitoring apparatus as set forth in Claim 15 wherein a bulk connection of said third transistor and a bulk connection of said fourth transistor are coupled to a positive supply voltage.

17. The battery monitoring apparatus as set forth in Claim 16 wherein a bulk connection of said seventh transistor and a bulk connection of said eighth transistor are coupled to said sources of said third and fourth transistors.

18. The battery monitoring apparatus as set forth in Claim 17 wherein a drain current of said fifth transistor and a drain current of said seventh transistor are combined to produce a first composite current.

19. The battery monitoring apparatus as set forth in Claim 18 wherein a drain current of said sixth transistor and a drain current of said eighth transistor are combined to produce a second composite current.

20. The battery monitoring apparatus as set forth in Claim 19 further comprising a current difference detection circuit capable of detecting a current difference in said second and first composite currents and generating an output voltage proportional to said current difference.